PK8211K 2.0MP Product Brief

The PK8211K has excellent noise performance for low light condition and high dynamic range support by 3-exp line based HDR mode upto 120dB

The PK8211K enables the smallest and most power-efficient viewing camera modules by consuming less than 150mW at the 30fps @3-exp HDR. The low power consumption and low noise performance enable front-view, rear-view, surround-view and IP cameras with excellent image quality.

The 120dB HDR implemented by using 3 exposure staggered output method. The HDR image shows no saturation or loss of shadow detain in situations of dramatic contrast such as when entering or exiting tunnels.

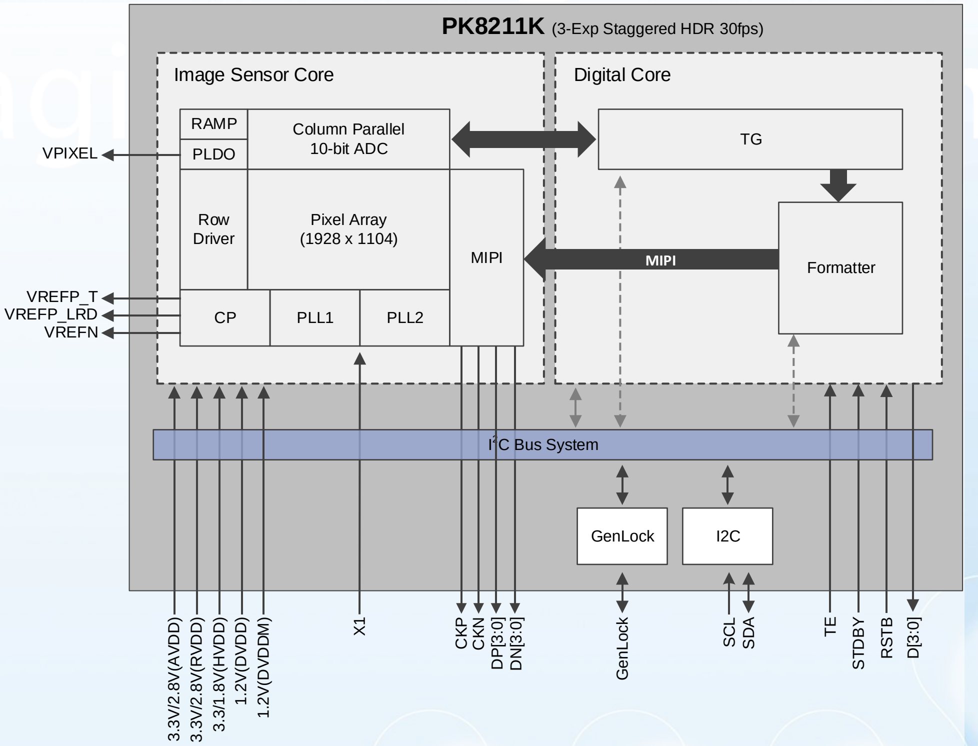
Applications

- Front/Rear View Camera
- 360° Surround View Monitoring System (SVM)
- Security (IPC, Analog)

Product Features

- 120dB HDR with line interleaving 3 staggered output
- Low fixed pattern noise of 2.8um BSI Pixel
- Separate RGB bayer output format
- Auto black level compensation support
- Programmable frame size, window size, and exposure
- Low shutter mode support up to 3.75fps
- External synchronization support (Genlock)
- Software reset mode support
- I^2C Interface support

Functional Block Diagram



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PIXELPLUS

Technical Specifications

Parameter	Typical value
Pixel size	2.8 um x 2.8 um
Effective pixel array	1924(H) x 1084(V)
Effective image area	5.3872 mm x 3.0352 mm
Optical format	1/2.92 inch
Input clock frequency	27 MHz
Output interface	MIPI serial interface with 1/2/4 lane (MIPI lane number can be selected as to exposure mode & frame rate)
Max. frame rate	90fps @ 1-exp SDR 45fps @ 2-exp HDR 30fps @ 3-exp HDR
Dark signal	TBD e/sec
Sensitivity	6.0 V/Lux·s
Power supply	HVDD : 1.8 ~ 3.3 V
	AVDD : 3.3/2.8 V
	DVDD : 1.2 V
	DVDDM : 1.2 V
Power consumption Active / Standby @ 30fps,2-exp	DVDD : 42.0 mA / 1 uA AVDD : 29.7 mA / 45 uA HVDD : 1.0 mA / 50 uA
Operating temp.	-40 ~ 85 °C (Ambient)
Max. dynamic range	120 dB
SNR	TBD dB
Package type	CSP 40ball

CSP Ball MAP

- Chip size : 6187um * 4022um, 40 ball

Ball Configuration (Top View)

CSP Ball Description

Ball	NAME	I/O Type	pullup/ pulldown	Ball Description
A1	AGND	P	-	Analog GND
A2	AVDD	P	-	Anallog VDD 2.8V
A3	RVDD	P		Analog VDD 2.8V
A4	TE	I	-	Chip test mode enable
A5	DVDD	P	-	Digital(Core) VDD 1.2V DC
A6	DGND	P	-	Digital(Core) GND
A7	AVDD	P	-	Anallog VDD 2.8V
A8	AGND	P	-	Analog GND
B1	RGND	P	-	Analog GND
B2	VREFN	P	-	NCP output. It should be tied with nearby AGND by both 1uF bypass capacitors.
B3	HGND	P	-	IO GND
B4	DVDDM	P	-	MIPI VDD 1.2V DC
B5	HVDD	P	-	IO VDD 3.3V DC
B6	D1	O	-	Digital Output bit 1
B7	D0	O	-	Digital Output bit 0
B8	VPIXEL	P	-	PCP output. It should be tied with nearby AGND by both 1uF bypass capacitors.
C1	DVDD	P	-	Digital(Core) VDD 1.2V DC
C2	DGND	P	-	Digital(Core) GND
C3	RSTB	I	pullup	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
C4	CKN	O	pulldown	MIPI Clock Negative Output
C5	CKP	O	pulldown	MIPI Clock Positive Output
C6	DGNDM	P	-	MIPI GND
C7	D3	O	-	Digital Output bit 3
C8	GENLOCK	BIO	pulldown	External Frame sync input. Slave chip can receive the external frame sync signal from master chip/External Frame sync output. Master chip can output the external frame sync signal through this pad to synchronize all digital outputs of two or more chips
D1	VREFP_T	P	-	PCP output.. It should be tied with nearby AGND by both 1uF bypass capacitors.
D2	SDA	BIO	pullup	2-wire serial interface clock, SDA line is pulled up to HVDD by off-chip resistor.
D3	DP3	O	pulldown	MIPI DP3 Output
D4	DN2	O	pulldown	MIPI DN2 Output
D5	DP1	O	pulldown	MIPI DP1 Output
D6	DN0	O	pulldown	MIPI DN0 Output
D7	DGND	P	-	Digital(Core) GND
D8	D2	O	-	Digital Output bit 2
E1	VREFP_LRD	O	-	PCP output. It should be tied with nearby AGND by both 1uF bypass capacitors
E2	SCL	BIO	pullup	2-wire serial interface data, SCL line is pulled up to HVDD by off-chip resistor.
E3	DN3	O	pulldown	MIPI DN3 Output
E4	DP2	O	pulldown	MIPI DP3 Output
E5	DN1	O	pulldown	MIPI DN1 Output
E6	DP0	O	pulldown	MIPI DP0 Output
E7	DVDD	P	-	Digital(Core) VDD 1.2V DC
E8	XI	I	-	Master clock input pad